# Jeonghyun Park

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Portfolio : https://alexist2623.github.io/index.html

## EDUCATION

**Seoul National University** Mar. 2018 – Aug. 2024
- B.S. in Electrical and Computer Engineering, Physics — Summa Cum Laude, GPA 3.77/4.0

## SKILLS

**Programming Languages:** Verilog/SystemVerilog, C/C++, ARMv8 Assembly, Python, TCL, MATLAB
**Tools:** Xilinx Vivado/Vitis, Cadence OrCAD, ANSYS SIwave/HFSS/EDT, LTSpice
**Measurement Equipment:** Oscilloscope, Spectrum Analyzer
**Communication Protocols:** AXI4, Camera Link, HDMI, DVI, UART, RS232, SPI, TCP
**Techniques:** CDC, SI Validation, Soldering

## PROFESSIONAL EXPERIENCE

**Research Assistant**
Quantum Information and Quantum Computing Lab, Seoul National University Mar. 2023 – Apr. 2025
- Led development of Xilinx RFSoC based real-time quantum computer controller from scratch that increased pulse-sequence depth by 1,000 times and integrated eight external RF chips to a single chip. (Details)
- Designed a double-buffered DDR4 SDRAM-based true-arb 1 GSPS AWG microarchitecture with row-aligned DRAM allocation, achieving deterministic worst-case latencies of 900 ns (1 ch) and 2.16 us (8 ch).
- Modeled DDR4 latency as a function of AWG buffer size, which achieved accuracy within 5 % of measured values.
- Removed AXI4 stalls by developing a multi-threaded microarchitecture of DMA IP and an interrupt-driven flow-control scheme, which achieved 3.2 GB/s, 160 MB/s respectively.
- Developed multi-processor (ARM Cortex A53) bare-metal firmware (LWIP server, binary loader, and monitor) which ran continuously for months.
- Achieved -27 dB RF reflection, 100 dB A/D isolation of a mixed-signal 8-layer PCB. Improved the reflection by 10 dB via optimizing a stripline-SMA transition through ANSYS HFSS. (Details)
- Verified 1 GHz signal integrity of FMC VITA57.1/57.4 router via ANSYS SIWave. It is deployed in Camera Link frame grabber, photon count and RF switch control. (Details)
- Led development of EMC-cosidered, low-noise DAC sub-system (TI DAC81416). Verified 50 MHz signal integrity of 3m shielded cable between FPGA and DAC through IBIS and ANSYS EDT. (Details)
- Automated Vivado IP integration (block diagram generation and AXI address assignment) cutting setup time from hours to 5 minutes.

**Research Assistant**
Quantum Information and Quantum Computing Lab, Seoul National University Feb. 2020 – Jan. 2021
- Tested an AD9910 EVB custom with Arty S7 through custom QSPI RTL design.

## PROJECTS

**Image Display/Frame Grabber on MPSoC (Capstone) (Details)** Feb. 2024 – Jun. 2024
- Developed a custom double buffer-based 60FPS DVI IP leveraging a GTH transceiver.
- Developed a custom real time 60FPS Camera Link frame grabber IP using 7:1 SERDES and DDR4 SDRAM.

## SCHOLARSHIP

**Presidential Science Scholarship, Korea Student Aid Foundation(KOSAF)** Mar. 2018 – Aug. 2024
- Selected as one of 147 STEM undergraduates nationwide (top 0.1%) with a cumulative award of CAD $44,000.

## LANGUAGE

**IELTS Academic Overall Band 6.5** May. 2025